In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1   1.   (Original) A field programmable device (FPD) implementing
2   a circuit logic containing a first base sequential element to be
3   clocked by a first circuit clock and a second base sequential
4   element to be clocked by a second circuit clock, said FPD
5   comprises:
6   a first modified sequential element to receive a global clock
7   and said first circuit clock, said first modified sequential
8   element containing said first base sequential element, said global
9   clock being connected to a clock input of said first base
10 sequential element, said first base sequential element
11 transitioning to a next state only after occurrence of a transition
12 on said first circuit clock and transition to said next state being
13 timed according to said global clock; and
14   a second modified sequential element to receive said global
15 clock and said second circuit clock, said second modified
16 sequential element containing said second base sequential element,
17 said global clock being connected to a clock input of said second
18 base sequential element, said second base sequential element
19 transitioning to a next state only after occurrence of a transition
20 on said second circuit clock and transition to said next state
21 being timed according to said global clock.

1   2.   (Original) The FPD of claim 1, wherein timing the
2   transitions of said first base sequential element and said second
3   base sequential element according to said global clock avoids
4   problems due to any substantial skew present between said first
5   circuit clock and said second circuit clock.

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1   3.   (Original) The FPD of claim 2, wherein the clock period
2 of said global clock is more than the maximum skew between said
3 first circuit clock and said second circuit clock.

1   4.   (Original) The FPD of claim 2, wherein said FPD is used
2 to validate a logic design of said circuit logic.

1   5.   (Original) The FPD of claim 1, wherein said first
2 modified sequential element further comprises:
3   a first multiplexor selecting an output of said first base
4 sequential element if a select input to said first multiplexor is
5 at a first logic level, and selecting a data input if said select
6 input is at a second logic level, wherein said data input is
7 designed to be an input to said first base sequential element
8 according to said circuit logic, said multiplexor providing said
9 output as an input to said first base sequential element; and
10   a detect block generating said select input such that said
11 select input changes from said first logic level to said second
12 logic level after occurrence of a transition on said first circuit
13 clock.

1   6.   (Original) The FPD of claim 5, wherein said detect block
2 is shared by said first modified sequential element and said second
3 modified sequential element.

1   7.   (Original) The FPD of claim 1, wherein said FPD comprises
2 a FPGA.

1   8.   (Original) An apparatus implementing a circuit logic in a
2 field programmable device (FPD), said circuit logic containing a
3 first base sequential element to be clocked by a first circuit

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4   clock and a second base sequential element to be clocked by a
5   second circuit clock, said apparatus comprising:
6   means for transitioning said first base sequential element to
7   a next state after the occurrence of a transition on said first
8   circuit clock, transition to said next state of said first base
9   sequential element being timed according to a global clock; and
10   means for transitioning said second base sequential element to
11 a next state after the occurrence of a transition on said second
12 circuit clock, transition to said next state of said second base
13 sequential element being timed according to said global clock.

1   9.   (Original) A method of implementing a circuit logic in a
2   field programmable device (FPD), said circuit logic containing a
3   first base sequential element to be clocked by a first circuit
4   clock and a second base sequential element to be clocked by a
5   second circuit clock, said method comprising:
6   transitioning said first base sequential element to a next
7   state only after the occurrence of a transition on said first
8   circuit clock, transition to said next state of said first base
9   sequential element being timed according to a global clock; and
10   transitioning said second base sequential element to a next
11 state only after the occurrence of a transition on said second
12 circuit clock, transition to said next state of said second base
13 sequential element being timed according to said global clock.

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